Amendments to the Claims

Listing of Claims:

Claims 1-9 (canceled).

Claim 10 (currently amended). A circuit configuration for determining an average value of an input signal, comprising:

a signal input terminal for receiving the input signal and

a signal output terminal for outputting an output signal (g, Q_1 ... Q_{n+m}) indicating the average value of the input signal;

a comparator connected between said signal input terminal and said signal output terminal, said comparator having an output;

a counter or summing unit connected between said signal input and said signal output for averaging, said counter having an input connected to said output of said comparator;

a switching element connected in a feedback loop for selectively connecting a first reference signal or a second reference signal to an input of said comparator and activated by said output of said comparator for switching to [[a]] the first reference signal or [[a]] the second reference signal in dependence on an output signal at said output of said comparator;

said counter or summing unit having a reset input connected to receive a control signal, wherein the control signal and the input signal have at least one of a

common fundamental frequency, a common phase angle, and a constant phase relationship to one another.

Claim 11 (currently amended). The circuit configuration according to claim 10, wherein said comparator forms a functional unit of a sigma-delta modulator and said input of said counter or summing unit is connected to [[a]] said sigma-delta modulator.

Claim 12 (currently amended). The circuit configuration according to claim 11, wherein said sigma-delta modulator has an adding unit or a subtracting unit, an integrator and said comparator, and [[a]] said feedback loop from said output of said comparator to an input of said adding unit or subtracting unit.

Claim 13 (previously presented). The circuit configuration according to claim 10, wherein said counter or summing unit has a clock input connected to receive a clock signal with a predefined clock frequency.

Claim 14 (previously presented). The circuit configuration according to claim 13, wherein the input signal is band-limited and has a predefined limit frequency, and the clock frequency is a whole-number multiple of the limit frequency.

Claim 15 (currently amended). The circuit configuration according to ~~claim 10~~ claim 13, wherein the clock signal and the control signal have a temporally constant phase relationship to one another.

Claim 16 (currently amended). The circuit configuration according to claim 10, which comprises an output register, and wherein said counter or summing unit ~~or adding unit or counter~~ has an output connected to said output register.

Claim 17 (previously presented). The circuit configuration according to claim 16, wherein said output register has a control input for controlling a receipt of data, said control input receiving the control signal.